SCHOTTKY-BARRIER TUNNELING TRANSISTOR

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RELATED APPLICATIONS

This application is a Continuation-in-Part of the US Patent Application Serial No. 10/438,674, filed on May 15, 2003, titled "Schottky-Barrier Tunneling Transistor", the content of which is hereby incorporated by reference.

now U.S. Patent No. 6,744,111

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TECHNICAL FIELD

This application relates to a semiconductor device, specifically, a semiconductor transistor device suitable for analog and digital circuits.

BACKGROUND OF THE INVENTION

For more than 30 years, the integrated circuit industry has followed a dramatic path of shrinking device dimensions and increasing chip sizes, resulting in steadily increased performance and increased functionality. New generations of devices have appeared in every two to three years, following the so called "Moore's Law", with each new generation device approximately doubling logic circuit density, increasing performance by about 40%, and quadrupling the memory capacity comparing to the previous generation. The consistency of this advancement has led to an expectation that faster and more powerful chips will continue to be introduced on the same schedule in the foreseeable future.

The silicon semiconductor industry has charted a course for itself over the next 15 years, which attempts to continue the density and performance improvements of the past 40 years. The International Technology Roadmap for Semiconductor (ITRS) has forecasted that this device scaling and increased functionality scenario to continue until 2013, at which point the minimum feature size is projected to reach 32 nm and a single chip is expected to contain more than 10^{11} components.